

# Design of 4 bit Bidirectional Barrel Shifter based on Decoder and NMOS Transistor.

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**Abstract** - A Barrel shifter is a combinational logic circuit which is used to shift multiple binary data bits in a single cycle whereas the standard shift Left or Right registers utilize more than one clock cycle to shift multiple binary data bits. Barrel Shifter rotates binary numbers in a cycle such that empty spots are filled with the bits shifted off the other end. Barrel shifter is one of the most important data path elements and widely used in many key computer operations from address decoding to computer arithmetic, using basic operations like data shifting or rotation. Bidirectional barrel shifter can shift multiple binary data bits to right or left direction. Right/left shift operation is controlled by mode select control input signal. This paper presents design of the 4-bit bidirectional barrel shifter. The decoder and NMOS transistor array are used in the design. The proposed design is modelled in Verilog HDL and simulations of the same is obtained using Xilinx Vivado Design Suit 16.2.

Bidirectional barrel shifter can perform right shifting as well as left shifting operation.

## 2. PROPOSED BASIC BARREL SHIFTER:

The barrel shifter can shift multiple bits in a single cycle and is an important part of microprocessors. The right shifting operation is tabulated below in Table.1 where  $S_1, S_0$  are control lines,  $Y_3, Y_2, Y_1, Y_0$  are output data lines and  $I_0, I_1, I_2$  and  $I_3$  are input data lines. In right shift operation, 4 bit input data  $I_0, I_1, I_2, I_3$  shifted to right position by 0,1,2,3 bit position depending on logic levels at control inputs  $S_1, S_0$ .

**Table -1:** Right shift operation

Control lines	Outputs	Operation
<b>S1 S0</b>	<b>Y3 Y2 Y1 Y0</b>	--
0 0	I3 I2 I1 I0	No operation
0 1	I0 I3 I2 I1	1 bit right shift
1 0	I1 I0 I3 I2	2 bit right shift
1 1	I2 I1 I0 I3	3 bit right shift

**Key Words:** Barrel shifter, Bidirectional ,HDL, Simulators

## 1.INTRODUCTION

Data shifting or rotation is an important function of arithmetic operations, address decoding and coding techniques. A Barrel shifter is a combinational logic circuit having n inputs, n outputs and k select lines which controls the bit shift operation. Unidirectional barrel shifter allows data to be shifted to right or left direction. Bidirectional barrel shifter provides shifting in both directions. In microprocessor barrel shifter is incorporated as a part of ALU to provide fast data shifting operation. Barrel shifter can be implemented using conventional multiplexes, decoders, and logic gates. There are two common architectural layouts for barrel shifter, array barrel shifter and logarithmic barrel shifters. An array type barrel shifter can be implemented using decoder and NMOS transistors as switching element. Logarithmic barrel shifter can be implemented as a cascade of parallel 2x1 multiplexers. In this paper design of 4 bit Bidirectional barrel shifter is presented. First a 4 bit right shift barrel shifter is designed using single decoder and NMOS transistor array which is used as a crossbar switch network to pass input data bits to output. This barrel shifter can shift binary data to right direction only. Then with some modification a 4 bit Bidirectional barrel shifter is designed which uses two decoders and NMOS transistor array used as a crossbar switch network to pass input data bits to output. This new design of

The right shifting operation is tabulated in Table.1 can be implemented using Barrel shifter constructed using NMOS transistor array and 2-to-4 line Decoder circuit as shown in Fig.1 below. In this circuit NMOS transistor array is used as a crossbar switch network to pass input data bits to output. Two inputs A and B provides 4 possible output combination of D3,D2,D1 and D0 which controls the switching of the desired NMOS transistors.

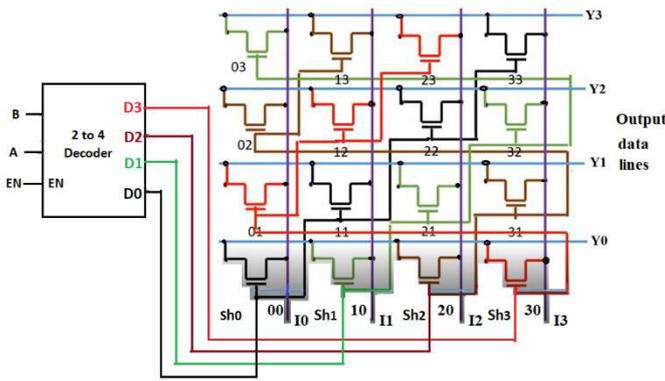


Fig.1 Barrel Shifter (Right Shift)

**3. WORKING:**

In above circuit 16 NMOS transistors are connected in crossbar switch network which passes 4 bit input binary data to output when transistors are ON. The ON/OFF switching of NMOS transistors in crossbar switch array is controlled by decoder output. Truth table describing functionality of the circuit is given in Table.2. When EN input to 2-to-4 line Decoder is '0' ,NMOS transistor switches are disabled and when EN input is at logic '1' NMOS transistor switches are ON.

**Table -2:** Right shift operation

Control Inputs	Decoder Output				Circuit Output	Operation
	D3	D2	D1	D0		
EN A B	Sh <sub>3</sub>	Sh <sub>2</sub>	Sh <sub>1</sub>	Sh <sub>0</sub>	Y <sub>3</sub> Y <sub>2</sub> Y <sub>1</sub> Y <sub>0</sub>	--
0 X X	0	0	0	0	- - - -	--
1 0 0	0	0	0	1	I <sub>3</sub> I <sub>2</sub> I <sub>1</sub> I <sub>0</sub>	No shift
1 0 1	0	0	1	0	I <sub>0</sub> I <sub>3</sub> I <sub>2</sub> I <sub>1</sub>	1 bit right shift
1 1 0	0	1	0	0	I <sub>1</sub> I <sub>0</sub> I <sub>3</sub> I <sub>2</sub>	2 bit right shift
1 1 1	1	0	0	0	I <sub>2</sub> I <sub>1</sub> I <sub>0</sub> I <sub>3</sub>	3 bit right shift

**4. BIDIRECTIONAL DATA SHIFTING:**

Bidirectional data shifting i.e. right or left shifting can be achieved in a single operation if three control lines S<sub>2</sub>,S<sub>1</sub>,S<sub>0</sub> are used as shown in Table. 3. When control line S<sub>2</sub> = 0 right shift operation takes place and when S<sub>2</sub> =1 left shift operation takes place.

**Table -3:** Right/Left shift operation (Bidirectional barrel shifter)

Control lines	Outputs	Operation
S <sub>2</sub> S <sub>1</sub> S <sub>0</sub>	Y <sub>3</sub> Y <sub>2</sub> Y <sub>1</sub> Y <sub>0</sub>	--

0 0 0	I <sub>3</sub> I <sub>2</sub> I <sub>1</sub> I <sub>0</sub>	No shifting
0 0 1	I <sub>0</sub> I <sub>3</sub> I <sub>2</sub> I <sub>1</sub>	1 bit right shift
0 1 0	I <sub>1</sub> I <sub>0</sub> I <sub>3</sub> I <sub>2</sub>	2 bit right shift
0 1 1	I <sub>2</sub> I <sub>1</sub> I <sub>0</sub> I <sub>3</sub>	3 bit right shift
1 0 0	I <sub>3</sub> I <sub>2</sub> I <sub>1</sub> I <sub>0</sub>	No shifting
1 0 1	I <sub>2</sub> I <sub>1</sub> I <sub>0</sub> I <sub>3</sub>	1 bit left shift
1 1 0	I <sub>1</sub> I <sub>0</sub> I <sub>3</sub> I <sub>2</sub>	2 bit left shift
1 1 1	I <sub>0</sub> I <sub>3</sub> I <sub>2</sub> I <sub>1</sub>	3 bit left shift

**5. PROPOSED BIDIRECTIONAL BARREL SHIFTER: (RIGHT/LEFT SHIFT)**

A 4-bit Bidirectional Barrel shifter capable of shifting 4 bit binary data input to Right or Left direction at the output is implemented using two 2-to-4 line Decoders and NMOS transistor crossbar switches as shown in Fig.2.below. In the given circuit 2-to-4 line Decoder circuit produces Active Low output where as Input is Active High.

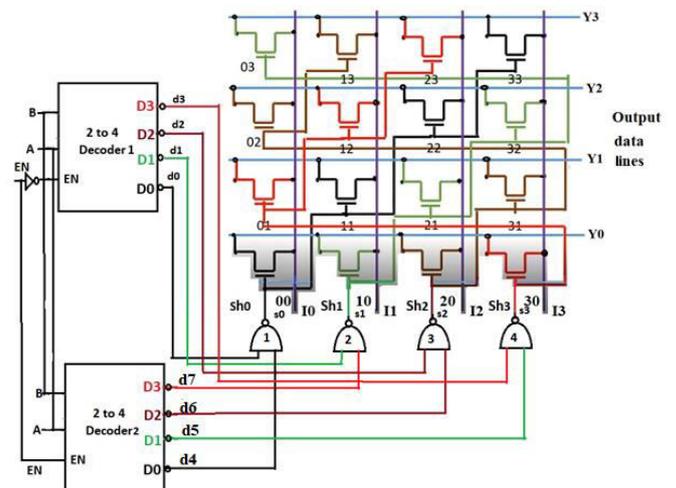


Fig.2. Decoder & NMOS Based Bidirectional Barrel Shifter

**5.1 OPERATING PRINCIPLE:**

The Bidirectional Barrel shifter circuit shown in above Fig. 2. can shift 4 bit Binary data input bits I<sub>0</sub>,I<sub>1</sub>,I<sub>2</sub> and I<sub>3</sub> to Right or Left direction depending on the status of Control inputs A,B and EN applied to 2-to-4 line Decoders used in the construction of the circuit. The circuit operation can be best illustrated by the function table given in Table 4.. The Enable input EN is connected to upper Decoder1 through NOT gate whereas it is directly connected to bottom Decoder2.

When Enable input EN is at logic'0', NOT gate output is at logic'1' and this enables the upper Decoder1. Whereas at the same time, logic'0' Enable input EN applied at the Enable pin of bottom Decoder2 will disable the Decoder2.Now output D<sub>0</sub>,D<sub>1</sub>,D<sub>2</sub> and D<sub>3</sub> of Decoder2 will be logic'1' state irrespective of control inputs A and B.So one input to NAND gate whose output is connected to Gate terminal of NMOS transistor will be always loic'1' and second input will be from Decoder1 output, therefore NAND gate acts as an inverter

producing logic'0' output and this will turn ON the desired NMOS transistors. Thus input data bits I0,I1,I2 and I3 will be shifted to Right direction 1 bit at a time.

When Enable input EN is at logic'1' status , logic'0' output at NOT gate will disable the upper Decoder1 and output D0,D1,D2 and D3 of Decoder1 will be logic'1' state irrespective of control inputs A and B which will be applied to one of the input to NAND gate. Second input to NAND gate will be output from Decoder2 and input data bits I0,I1,I2 and I3 will be shifted to Left direction 1 bit at a time.

T= 60 EN=1 A=1 B=0 Output Y=0100  
T= 70 EN=1 A=1 B=1 Output Y=1000



Fig.3(a). Simulation Output Waveforms for proposed Bidirectional barrel shifter

**4 Truth table of proposed Bidirectional barrel shifter:**

Control Inputs	Decoder O/P D <sub>3</sub> D <sub>2</sub> D <sub>1</sub> D <sub>0</sub>	Circuit Output	Operation
EN A B	Sh <sub>3</sub> Sh <sub>2</sub> Sh <sub>1</sub> Sh <sub>0</sub>	Y <sub>3</sub> Y <sub>2</sub> Y <sub>1</sub> Y <sub>0</sub>	--
0 0 0	1 1 1 0	I <sub>3</sub> I <sub>2</sub> I <sub>1</sub> I <sub>0</sub>	No shift
0 0 1	1 1 0 1	I <sub>0</sub> I <sub>3</sub> I <sub>2</sub> I <sub>1</sub>	1 bit right shift
0 1 0	1 0 1 1	I <sub>1</sub> I <sub>0</sub> I <sub>3</sub> I <sub>2</sub>	2 bit right shift
0 1 1	0 1 1 1	I <sub>2</sub> I <sub>1</sub> I <sub>0</sub> I <sub>3</sub>	3 bit right shift
1 0 0	1 1 1 0	I <sub>3</sub> I <sub>2</sub> I <sub>1</sub> I <sub>0</sub>	No shift
1 0 1	0 1 1 1	I <sub>2</sub> I <sub>1</sub> I <sub>0</sub> I <sub>3</sub>	1 bit left shift
1 1 0	1 0 1 1	I <sub>1</sub> I <sub>0</sub> I <sub>3</sub> I <sub>2</sub>	2 bit left shift
1 1 1	1 1 0 1	I <sub>0</sub> I <sub>3</sub> I <sub>2</sub> I <sub>1</sub>	3 bit left shift

**6. SIMULATION RESULTS AND DISCUSSION:**

The proposed Bidirectional barrel shifter is modeled in Verilog HDL. Test bench is written in Verilog HDL and simulation carried out on Xilinx's Vivado software design suit. Simulation output waveforms are shown in Fig.3(a) and Fig.3(b). for two set of 4 bit binary data.

Input I=1000  
T= 0 EN=0 A=0 B=0 Output Y=1000  
T= 10 EN=0 A=0 B=1 Output Y=0100  
T= 20 EN=0 A=1 B=0 Output Y=0010  
T= 30 EN=0 A=1 B=1 Output Y=0001  
Input I=0001  
T= 40 EN=1 A=0 B=0 Output Y=0001  
T= 50 EN=1 A=0 B=1 Output Y=0010

Input I=1011  
T= 0 EN=0 A=0 B=0 Output Y=1011  
T= 10000 EN=0 A=0 B=1 Output Y=1101  
T= 20000 EN=0 A=1 B=0 Output Y=1110  
T= 30000 EN=0 A=1 B=1 Output Y=0111  
Input I=0011  
T= 40000 EN=1 A=0 B=0 Output Y=0011  
T= 50000 EN=1 A=0 B=1 Output Y=0110  
T= 60000 EN=1 A=1 B=0 Output Y=1100  
T= 70000 EN=1 A=1 B=1 Output Y=1001



Fig.3(b). Simulation Output Waveforms for proposed Bidirectional barrel shifter.

**RTL Schematic diagram Bidirectional Barrel shifter:**

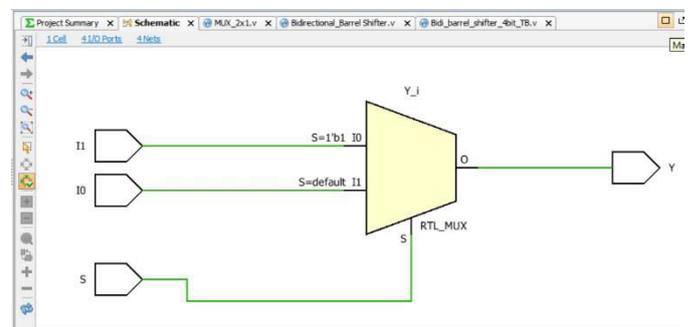


Fig.3(c) RTL Schematic diagram Bidirectional Barrel shifter.

**3. CONCLUSIONS:**

Hence proposed 4-bit Bidirectional Barrel Shifter is designed using Decoder and NMOS Transistor array. In this design two units of 2-to-4 line decoder circuit and 16 NMOS transistor connected as crossbar switch are used. The functionality of proposed 4-bit Bidirectional Barrel Shifter is verified by simulation done using Xilinx Vivado software design suit.

The output waveforms obtained in simulation shows the satisfactory results. The core can be used to design for further designs of 16-bit , 32-bit and so on .

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